REMARKS

Claims 1-31 were pending in the application. By this paper, Applicant has cancelled Claim 18 without prejudice, amended Claims 1, 5, 6, 8, 9, 14, 19, 20, 25, 26, 28 and 29, and added new Claims 32-41. Accordingly, Claims 1-17 and 19-41 are presented herein for examination.

Drawing Objections

Per Pars. 3-4 of the Office Action, the relevant drawings have been amended (a revised set included herewith) to include the missing or erroneous reference numbers. Copies of the Figures with changes marked in red ink are also included herewith for the Examiner's convenience.

Furthermore, Applicant notes that Fig. 33 as previously on file is in error as to its content. As will be noted, the text of the specification as filed (see pages 20-22) does not match the content of Fig. 33. Accordingly, Applicant submits herewith a new Fig. 33 that accurately reflects the substantive discussion of the text. Applicant notes that (i) the general content of Fig. 33 is also reflected in U.S. Patent Application Serial No. 09/418,663 entitled "Method And Apparatus For Managing The Configuration And Functionality Of A Semiconductor Design" filed October 14, 1999, which was incorporated by reference in its entirety into the present application at time of filing; and (ii) the aforementioned textual discussion of Fig. 33 provides complete support for the new Fig. 33 as presented herein. Hence, Applicant submits that no new matter is entered by way of these amendments.

Applicant respectfully requests that the requirement for "red ink" changes to Fig. 33 be held in abeyance, since the entirety of Fig. 33 has been changed as reflected on the new Fig. 33 submitted herewith.

Hence, Applicant submits that all objections to the drawings have been overcome.

Objections to Appendices

Per Par. 5 of the Office Action, Applicant has herein (i) amended the specification to delete the previously included computer code and related materials of Appendices I-XII from the

textual portion of the specification, (ii) submitted the above referenced code and materials as part of Compact Disc, and (iii) amended the specification to include a proper statement of incorporation by reference therein of the Compact Disc pursuant to 37 C.F.R. §1.52 and 1.77(b)(4).

Applicant submits that these actions overcome the Examiner's objections in this regard.

Claim Objections and Rejections under §112

Per Pars. 7-10 of the Office Action, Claims 5, 6, 9, 10, 19, 28 and 29 were either objected to or rejected under 35 U.S.C. §112. These claims (with the exception of Claim 10) have been amended herein to correct editorial errors, make the claims clearer, or provide sufficient antecedent basis as applicable, and overcome the Examiner's objections and rejections.

Regarding Claim 10, it states:

> *"10. The processor of Claim 8, wherein said optimized instruction set also comprises at least one extension instruction adapted to perform a predetermined function, said processor further comprises an extension logic unit adapted to execute said at least one extension instruction."*

Hence, Applicant respectfully submits that Claim 10 contains proper antecedent basis for the term "said at least one extension instruction".

Accordingly, Applicant submits that these amendments overcome the Examiner's objections and rejections.

§102 Rejections

Per Par. 11 of the Office Action, Claims 1-11, 14-17, and 19-26 were rejected under 35 U.S.C. 102(e) as being anticipated by Schlansker, et al. (U.S. 6,408,428; hereinafter "Schlansker").

By this paper, Applicant has amended independent Claims 1, 8, 14, 19, 20, 25 and 26 to overcome these rejections, as discussed below.

Claims 1, 8, 14, 19, 20, and 25 – Claims 1, 8, 14, 19, 20, and 25 have been amended herein to include limitations relating to determination of the static frequency of instruction types. Support for this limitation is found throughout the specification, including *inter alia* at page 12, line 25 through 31 of the specification as filed.

Applicant submits that Schlansker neither teaches nor suggests the determination of static frequency of each of a plurality of instruction types as recited in Applicant's claimed inventions. Rather, Schansker uses the term "static" to refer to combinations of "operation groups", as stated clearly at Col. 65, lines 40-51 of Schansker:

> "*FIG. 18 is a flow diagram illustrating a process of selecting custom templates from operation issue statistics. The process begins by extracting usage statistics from a scheduled application program 700. This is done by mapping the scheduled opcodes of an instruction back to their operation groups as shown in step 702. The process then generates a histogram of combinations of operation groups from the program as shown in step 704.*
>
> *A **static** histogram records the frequency of **static occurrences of each combination within the program** and may be used to optimize the static codesize.*" {Emphasis added}

Hence, Schlansker teaches the use of a compiler to generate an instruction set for a candidate architecture; instruction statistics are gathered to determine relationships between instructions during operation of the program. These operation statistics are used to enable subsequent iterations of the hardware design to make use of these relationships. Hence, Schlansker teaches iteratively refining the hardware design of a processor based on operational instruction issue statistics. In contrast, Applicant's claimed invention of Claims 1, 8, 14, 19, 20, and 25 determines the static frequency of instruction types within an existing code set in order to identify portions of the code which can be "compressed" to reduce code size. No iterative modification of the hardware design based on operational statistics is performed by Applicant's invention as taught in Schlansker. Hence, Schlansker cannot be considered to anticipate Applicant's claimed invention(s) as presented herein, since it does not explicitly or inherently teach a determination of the static or non-operational frequency of instruction types within the code set.

Furthermore, Schlansker's invention teaches away from Applicant's invention; see, e.g., page 13, line 30 through page 14, line 5 of Applicant's specification:

> *"Fig. 2 illustrates one exemplary compressed encoding structure 200 using the core instruction set from a pipelined RISC processor (i.e., the ARC™ core produced by the Applicant herein). The instruction structure was constrained to only use 2 extension instruction slots, as only 2 slots are currently available in the aforementioned processor architecture. It will be appreciated, however, that other numbers of instruction slots and encoding structures may be used as compatible with the host processor's architecture. See, for example, the discussion relating to Table 1 herein."*

Hence, while Applicant's invention can be used with a varying number of instruction slots, and foregoing passage (and citation of herein) should in no way be considered to be a surrender of such scope, the foregoing passage does clearly indicate that Applicant's invention is intended to be adapted to an existing processor architecture; i.e., the architecture is not iteratively revised based on the aforementioned determination of static frequency of instruction types. Schlansker's operational determination of usage statistics would have literally no utility for compressing code for an existing architecture as in Applicant's invention. Therefore, one could not combine the teachings of Schlansker with any other cited art to produce Applicant's claimed invention(s).

Hence, based on the foregoing, Applicant respectfully submits that Schlansker cannot anticipate or render obvious Applicant's inventions of Claims 1, 8, 14, 19, 20, and 25, and such claims therefore define patentable subject matter.

Claim 26 – Claim 26 has been amended to include limitations relating to the recited pipelined digital processor being extended (i.e., having extension instructions and/or hardware determined at least in part by selections made by a user), and deriving the compressed instruction set derived at least in part from said base and extension instruction sets. Support for these amendments can be found at, *inter alia*, page 13, line 30 through page 14, line 5 of the specification as filed (cited above). Schlansker in no way teaches or suggests creation of a compressed instruction set based at least in part on one or more extension instructions. Schlansker, arguendo, at best teaches creation of additional "templates" or hardware based on the results of its operational statistics analysis. Applicant respectfully submits that this is a far cry

from creating a compressed instruction set based (at least in part) on these extensions. No "compression" of the extension templates or hardware of Schlansker is performed that Applicant can divine.

Based on the foregoing, Applicant submits that independent Claim 26 distinguishes over the art of record, and overcome the Examiner's rejections.

§103 Rejections

The Examiner rejected Claims 12-13 and 27-31 under 35 U.S.C. §103(a) as being unpatentable over Schlansker. Applicant submits that since each of these claims depends directly or indirectly from one of the independent claims listed above, each of these dependent claims are non-obvious over the art of record as well.

New Claims

By this paper, Applicant has added new Claims 32-41, each of which are supported by the specification as filed. Applicant submits that each of these new Claims distinguish over the art of record (including Schlansker), and are also in condition for allowance.

Hence, in summary, Applicant submits that Claims 1-17 and 19-41 and are in condition for allowance. Applicant respectfully requests that the Examiner pass this case to issuance at the earliest opportunity.

Other Remarks

Applicant hereby specifically reserves the right to prosecute claims of different or broader scope in a continuation or divisional application.

Applicant notes that any claim cancellations or additions made herein are made solely for the purposes of more clearly and particularly describing and claiming the invention and responding to the aforementioned restriction election, and not for purposes of overcoming art or for patentability. The Examiner should infer no (i) adoption of a position with respect to patentability, (ii) change in the Applicant's position with respect to any claim or subject matter of the invention, or (iii) acquiescence in any way to any position taken by the Examiner, based on such cancellations or additions.

Furthermore, any remarks made with respect to a given claim or claims are limited solely to such claim or claims.

If the Examiner has any questions or comments that may be resolved over the telephone, he/she is requested to call the undersigned at (858) 675-1670.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

Dated: August 2, 2004

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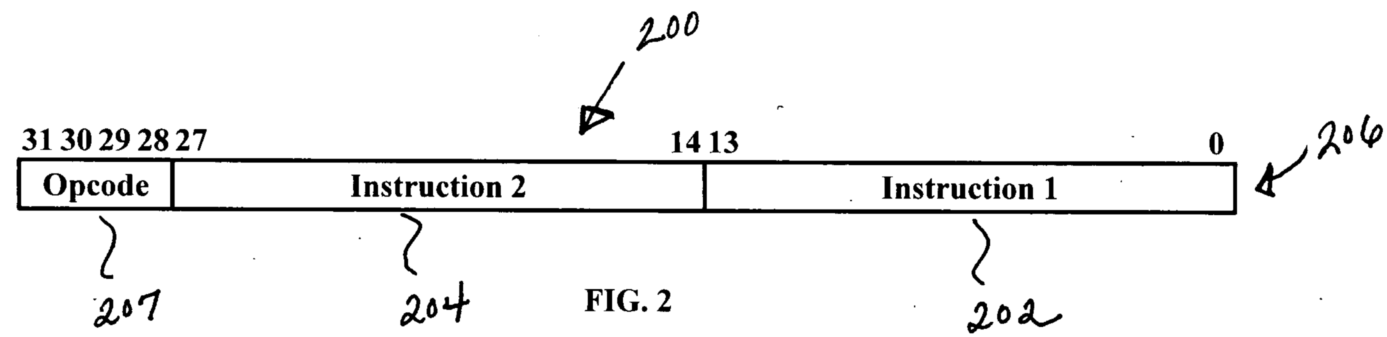

FIG. 2

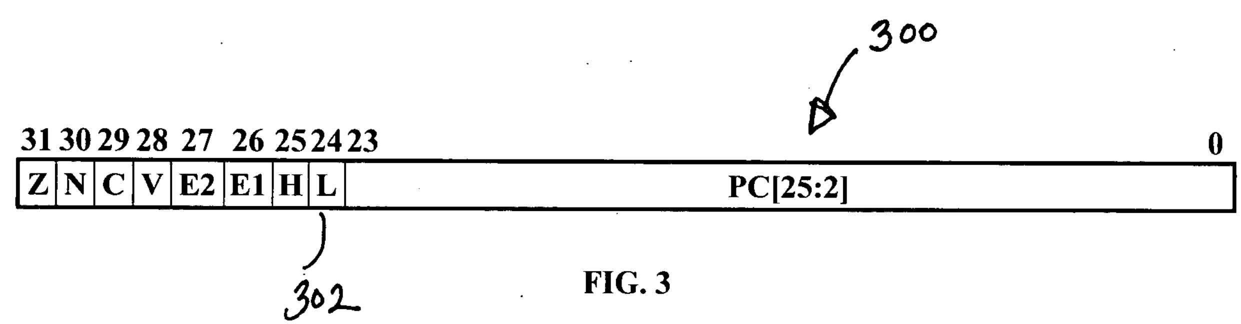

FIG. 3